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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/671,678	09/29/2003	Yasushi Aoki	8022-1060	8269

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EXAMINER	
NGUYEN, HAI L	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 03/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/671,678	AOKI, YASUSHI	
	Examiner	Art Unit	
	Hai L. Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *11-13* is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Applicant's Letter

1. The response letter received on 01/19/05 has been received and entered in the case. Applicant's arguments with respect to the prior art rejections by the previous office action mailed on 10/19/2004 have been fully considered and found persuasive, as such, the prior art rejections have been withdrawn. A new action on the merits appears below.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claim 9 is rejected under 35 U.S.C. 102(e) as being anticipated by Feldman (US 6,781,445; previously cited).

Feldman discloses in Figs. 4-6 an integrated circuit comprising an inherent logic circuit (not shown) developing first and second sinusoidal signals (VIN+, VIN-) whose phases are different by 180 degrees; and a differential output circuit (420, 430, 440 - 480) responsive to the first and second sinusoidal signals to develop first and second complementary output signals (VOUT-, VOUT+) on first and second outputs, respectively, wherein the differential output circuit includes an inductive element (480) connected between the first and second outputs.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Feldman in view of Barnes (US Pat. 6,404,229), and further in view of Llewellyn (US Pat. 6,724,248).

With regard to claims 1-4, Feldman discloses in Figs. 4-6 a differential circuit comprising a first input (at node between 420 and 440) receiving a first input signal; a second input (at node between 430 and 450) receiving a second input signal complementary to the first input signal; a first N-channel transistor (440) having a source connected to the first input, a gate receiving a power supply potential (435, column 5 lines 61-65), and a drain connected to the first output (445); a second N-channel transistor (450) having a source connected to the second input, a gate receiving the power supply potential, and a drain connected to the second output (455); a first P-channel transistor (460) having a source receiving the power supply potential, and a drain connected to the first output; and a second P-channel transistor (470) having a source receiving the power supply potential, and a drain connected to the second output. Figs. 4-6 of Feldman shows a circuit meeting all of the claimed limitations except that a first P-channel transistor having a gate connected to the first output instead of the second input, a second P-channel transistor having a gate connected to the second output instead of the first input, and an inductor element (480) instead of the resistor connected between the

first and second outputs. Barnes teaches in Figs. 1-2 a differential circuit having a first P-channel transistor (15) having a source receiving the power supply potential (Vdd), a gate connected to the second input (B) through the first N-channel transistor (21), and a drain connected to the first output (D); and a second P-channel transistor (16) having a gate connected to the first input (A) through the second N-channel transistor (20) and a drain connected to the second output (C). Therefore, it would have been obvious to one of ordinary skill in the art at the time of applicant's invention was made to change of the structural connections of the gates of the P-channel transistors as taught by Barnes in the circuit of the prior art (Fig. 4 of Feldman) in order to improve the speed of the circuit. Furthermore, Llewellyn teaches in Figs. 1 a circuit having a load (180) connected between differential outputs (176, 178), wherein the load may be inductive, capacitive, resistive, or any combination thereof. Therefore, it would have been obvious to one of ordinary skill in the art at the time of applicant's invention was made to replace the inductor element with the resistor or any combination thereof as taught by Llewellyn in the circuit of the prior art in order to meet the specific condition of the particular application. Moreover, the transistors in Kawashima's circuit are MOSFETs instead of MISFETs as recited in the claim. However, it will be understood that the MOSFETs of Kawashima can be practiced with other types of transistors as well, including MISFETs (see column 1, line 28 through column 2, line 31 of Sato et al. US Pat. 4,984,201). It would have been obvious to one of ordinary skill in the art at the time of applicant's invention was made to use the transistors of the prior art with MISFETs, instead of MOSFETs, in order to meet the specific condition of the particular application.

6. Claims 5-8 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Feldman in view of Barnes.

With regard to claims 5, 6, and 10, note the above discussion with regard to claims 1-4.

With regard to claims 7 and 8, note the above discussion with regard to claims 1-4. Furthermore, the claimed limitation "a logic circuit developing first and second clock signals complementary to each other" is also met by the references (405-432 in Fig. 4 of Feldman).

Allowable Subject Matter

7. Claims 11-13 are allowed.

The prior art of record fails to disclose or fairly suggest an integrated circuit, as recited in claims 11 and 13, having specific structural limitations such as a logic circuit (1 in instant Fig. 5) developing first and second input signals (IT, IB) complementary to each other, wherein the logic circuit includes a first pull-up N-channel MISFET (11) used for pull-up of the first input signal, and a second pull-up N-channel MISFET (13) used for pull-up of the second input signal, and being configured in combination with the rest of the limitations of the base claims and any intervening claims.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hai L. Nguyen whose telephone number is 571-272-1747

and Right Fax number is 571-273-1747. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The official fax phone number for the organization where this application or proceeding is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 571-272-1562.

9. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

HLN
March 2, 2005

TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800